REMARKS

Claims 7-14, 19, and 21-38 are pending in the application and are presented for reconsideration and further examination in view of the foregoing amendments and following remarks. Claims 9, 12-14, and 17 have been previously withdrawn from consideration by the Examiner as being drawn to a non-elected species.

In the outstanding Office Action the amendment filed July 8, 2004 was found to be non-responsive and has not been entered because it fails to conform to the provisions of MPEP 714.03. Specifically, the Examiner stated that the reply does not clearly point out the patentable novelty which Applicants think the amended claims present in view of the state of the art disclosed by the references cited, nor have Applicants shown how the amendments avoid the references.

By this Reply the patentable novelty of claims 19, 21-23, and 31 is discussed with regard to the amendment filed July 8, 2004. Arguments regarding claims 7, 8, 10, 11, 24-30, and 32-38 have been previously presented in the amendment filed April 2, 2004.

These amendments were not made to distinguish over any cited art. Therefore, the amendments to claims 19, 21-23, and 31 have not narrowed the scope of the claims within the meaning defined in Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., 535 U.S. 722 (2002). Applicants submit that amended claims 19, 21-23, and 31 are generic and/or linking claims read on the elected invention. However, Applicants respectfully request that claims 7, 8, 10, and 11 be examined along with the elected invention.

PATENTABLE NOVELTY

Claim 19

Claim 19 has been amended *inter alia*, to clarify that a film is laminated on one of a substrate having discrete solder bumps thereon or a semiconductor chip having an active surface thereon.

In contrast, the cited Akhavain et al. patent discloses at col. 4, lines 18-35 how a patterned photoresist layer 12e, interconnect member 12, input/output pads 12d, and solder paste 12f' are formed.

Applicants respectfully submit that in the presently claimed invention the solder bumps must necessarily be present on the substrate or the active surface must necessarily be present on the semiconductor chip before the film is laminated thereon so as to give meaning to the preamble term "*...in sequence.*"

In contrast, in the method disclosed in the Akhavain et al. patent the film must necessarily be applied to the substrate before solder past 12f' can be placed into the holes formed therein and similarly before the solder paste can be subjected to a high temperature to form fillets 12f.

Applicants respectfully submit that the method steps as disclosed in the Akhavain et al. patent are not arranged as required by claim 19 and therefore the Akhavain et al. patent does not anticipate nor render unpatentable the currently claimed method. Applicants therefore submit that claim 19 is patentable over the Akhavain et al. patent. Accordingly, reconsideration is respectfully requested.

Claim 21

Claim 21 has been amended *inter alia*, to clarify that a portion of an encapsulant is coated on one of a film or a substrate.

In contrast, the cited Akhavain et al. patent discloses at col. 4, lines 18-64 how a patterned photoresist layer 12e interconnect member 12, input/output pads 12d, and solder paste 12f' are formed.

Applicants respectfully submit that in the presently claimed invention the solder bumps must necessarily be present on the active surface of the semiconductor chip before a portion of an encapsulant is coated on one of the film or a substrate so as to give meaning to the preamble term "... *in sequence.*"

Applicants respectfully submit that Akhavain et al. nowhere discloses laminating a film on an active surface of a semiconductor chip having discrete solder bumps thereon. To the contrary, Akhavain et al. discloses that its stencil is laminated to the integrated circuit in order to facilitate thereafter fabricating the solder bumps. Applicants therefore submit that claim 21 is patentable over the Akhavain et al. patent taken alone or in combination. Accordingly, reconsideration is respectfully requested.

Claim 22

Claim 22 has been amended *inter alia*, to correct a minor informality. However, similar to claims 19 and 21, the recited method steps are performed in the particular sequence therein claimed. More particularly, a claim 22 recites performing, **in sequence**, the steps of laminating, coating, placing, curing, and reflowing.

In contrast, the cited Gutierrez et al. patent discloses at col. 5, lines 28-35 that a component is formed by performing, in sequence, the steps of: affixing, reflowing, dispensing, placing, and curing.

Applicants respectfully submit that the method steps as disclosed in the Gutierrez et al. patent are not arranged as required by claim 22 and therefore the Gutierrez et al. patent does not anticipate nor render obvious the currently claimed method. Applicants therefore submit that claim 22 is patentable over the Gutierrez et al. patent and accordingly, reconsideration is respectfully requested.

Claims 23 and 31

Claims 23 and 31 have been amended *inter alia*, to clarify that a semiconductor chip is provided having an active surface with a plurality of solderable contact pads; and that a first portion of an encapsulant is applied to one of at least a portion of the printed circuit substrate surface or at least a portion of the active surface of the semiconductor chip. Additionally, the first portion of the encapsulant comprises a particular chemical composition selected so as to not adversely affect properties of a second portion of the encapsulant.

In contrast, the cited Akhavain et al. patent discloses at col. 4, lines 18-64 how a patterned photoresist layer 12e interconnect member 12, input/output pads 12d, and solder paste 12f' are

formed. In further contrast, the cited Gutierrez et al. patent discloses at col. 5, lines 28-35 that a component is formed by performing, in sequence, the steps of: affixing, reflowing, dispensing, placing, and curing.

Applicants respectfully submit that in the presently claimed invention at least a portion of the printed circuit substrate or at least a portion of the active surface of the semiconductor chip must necessarily be present before a portion of an encapsulant is applied so as to give meaning recited steps.

Applicants respectfully submit that neither the Akhavain et al. nor Gutierrez et al. disclose applying a first portion of an encapsulant to at least a portion of a printed circuit substrate surface or at least a portion of an active surface of a semiconductor chip. Applicants respectfully submit that the method steps as disclosed in the Akhavain et al. and Gutierrez et al. patents are not arranged as required by claims 23 and 31 and therefore the references do not anticipate nor render obvious the currently claimed method. Applicants therefore submit that claim 23 and 31 are patentable over the Akhavain et al. and Gutierrez et al. patents taken alone or in combination. Accordingly, reconsideration is respectfully requested.

CONCLUSION

In light of the foregoing, Applicants submit that the application is in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicant respectfully requests that the Examiner contact the undersigned attorney if it is believed that such contact will expedite the prosecution of the application.

Respectfully submitted,

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